What is claimed is:

[Claim 1] 1. A method, comprising:

(a) providing a substrate;

(b) forming a first single-crystal layer on a top surface of said substrate;

(c) forming a second single-crystal layer on a top surface of said first single-crystal layer;

(d) forming one or more devices in said second single-crystal layer;

(e) forming a trench in said second-single crystal layer to form a single-crystal island containing said one or more devices, said first single-crystal layer exposed in a bottom of said trench; and

(f) removing said first single-crystal layer in order to separate said single-crystal island from said substrate.

[Claim 2] 2. The method of claim 1, wherein step (f) includes selectively removing said first single-crystal layer with respect to said second-single crystal layer.

[Claim 3] 3. The method of claim 1, wherein said substrate comprises silicon.

[Claim 4] 4. The method of claim 1, wherein said first single-crystal layer comprises Si_xGe_y, Si_xC_y or Si_xAs_y.

[Claim 5] 5. The method of claim 1, wherein said second single-crystal layer comprises silicon.

[Claim 6] 6. The method of claim 1, further including:

(g) after step (f) repeating steps (a) through (f) one or more times.

[Claim 7] 7. The method of claim 1, further including:

(g) after step (f) mechanical-chemical-polishing said substrate to expose a new top surface of said substrate; and

(h) after step (g) repeating steps (a) through (g) one or more times.

[Claim 8] 8. The method of claim 1, further including:

between steps (e) and (f), forming a spacer on a sidewall of said single crystal island.

[Claim 9] 9. The method of claim 1, wherein said one or more devices are independently selected from the group consisting of NFETS, PFETs, bipolar transistors, resistors and capacitors.

[Claim 10] 10. The method of claim 1, wherein step (d) further includes interconnecting said one or more devices to form an integrated circuit in said second-single crystal layer.

[Claim 11] 11. The method of claim 10, wherein said integrated circuit is a radio frequency identification circuit.

[Claim 12] 12. The method of claim 1, wherein said trench comprises one or more intersecting trenches.

[Claim 13] 13. A method, comprising:

(a) providing a single-crystal substrate;

(b) forming a buried single-crystal layer in said substrate;

(c) forming one or more devices in said a layer of said single-crystal substrate above said buried single-crystal layer;

(d) forming a trench in said layer of said single-crystal substrate above said buried single-crystal layer to form a single-crystal island containing said one or more devices, said buried single-crystal layer exposed in a bottom of said trench; and

(f) removing said buried single-crystal layer in order to separate said single-crystal island from said substrate.

[Claim 14] 14. The method of claim 13, wherein step (b) includes performing an ion implantation of Ge or As followed by performing a heat treatment.

[Claim 15] 15. A structure, comprising:

a substrate;

a first single-crystal island on a top surface of said substrate; and

a second single-crystal island on a top surface of said first single-crystal island, said second single-crystal island containing one or more devices or an integrated circuit.

[Claim 16] 16. The structure of claim 15, wherein said substrate comprises silicon, said first single-crystal island comprises Si_xGe_y, Si_xC_y or Si_xAs_y and said second single crystal island comprises silicon.

[Claim 17] 17. The structure of claim 15, wherein said first single-crystal island is selectively etchable with respect to said second-single crystal island.

[Claim 18] 18. The structure of claim 15, further including a spacer on sidewalls of said second single crystal island.

[Claim 19] 19. The method of claim 15, wherein said one or more devices are independently selected from the group consisting of NFETS, PFETs, bipolar transistors, resistors and capacitors.

[Claim 20] 20. The structure of claim 15, wherein said integrated circuit is a radio frequency identification circuit.